10/070013
JC ec'd PCT/PTO 28 FEB 2002

WHAT IS CLAIMED IS:

1. A radio frequency (RF) up-convertor with reduced local oscillator leakage, for modulating an input signal *x(t)*, comprising:
a synthesizer for generating mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;
a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said mixing signal φ_1 to generate an output signal $x(t)\ \varphi_1$; and
a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal $x(t)\ \varphi_1$ with said mixing signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

2. The radio frequency (RF) up-convertor of claim 1 wherein said synthesizer further comprises:
a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

3. The radio frequency (RF) up-convertor of claim 2 wherein said synthesizer further comprises:
a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

4. The convertor of claim 3, further comprising:
a closed loop error correction circuit.

5. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:
an error level measurement circuit for measuring an error in said output signal $x(t)\ \varphi_1\ \varphi_2$; and
a time-varying signal modification circuit for modifying a parameter of one of said mixing signals φ_1 and φ_2 to minimize said error level.

6. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a power measurement.

7. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a voltage measurement.

8. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a current measurement.

9. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the phase delay of one of said mixing signals φ_1 and φ_2.

10. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the fall or rise time of one of said mixing signals φ_1 and φ_2.

11. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said mixing signals φ_1 and φ_2.

12. The radio frequency (RF) up-convertor of claim 3 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where said mixing signals φ_1 and φ_2 can change with time in order to reduce errors.

13. The radio frequency (RF) up-convertor of claim 3, further comprising:

a DC offset correction circuit.

14. The radio frequency (RF) up-convertor of claim 13, wherein said DC offset correction circuit comprises:

a DC offset generating circuit for generating a DC offset voltage;

a summer for adding said DC offset voltage to an output of one of said mixers; and

a DC error level measurement circuit for modifying the level of said DC offset voltage to minimize error level.

15. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a power measurement circuit.

16. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a voltage measurement circuit.

17. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a current measurement circuit.

18. The radio frequency (RF) up-convertor of claim 1, further comprising:
a filter for removing unwanted signal components.

19. The radio frequency (RF) up-convertor of claim 18, where said filter comprises:
a filter for removing unwanted signal components from said $x(t)$ φ_1 signal.

C1 Cont

20. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are random.

21. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are pseudo-random.

22. The radio frequency (RF) up-convertor of claim 1, wherein said synthesizer uses a single time base to generate both mixing signals φ_1 and φ_2.

23. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are digital waveforms.

24. The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are square waveforms.

25. The radio frequency (RF) up-convertor of claim 3, further comprising:
a local oscillator coupled to said synthesizer for providing a periodic signal having a frequency that is an integral multiple of the frequency of said local oscillator signal being emulated.

26. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises a digital signal processor (DSP).

27. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises analogue components.

28. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal $x(t)\ \varphi_1$; and

a time-varying signal modification circuit for modifying a parameter of one of said mixing signals φ_1 and φ_2 to minimize said error level.

29. The radio frequency (RF) up-convertor of claim 1, where said synthesizer uses different patterns to generate signals φ_1 and φ_2.

31. A method of modulating a baseband signal $x(t)$ comprising the steps of:

generating mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi 1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

mixing said input signal $x(t)$ with said mixing signal φ_1; to generate an output signal $x(t)\ \varphi_1$; and

mixing said signal $x(t)\ \varphi_1$ with said mixing signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

32. An integrated circuit comprising the radio frequency (RF) up-convertor of claim 1.

WHAT IS CLAIMED IS:

1. A radio frequency (RF) up-convertor with reduced local oscillator leakage, for modulating an input signal *x(t)*, comprising:

a synthesizer for generating ~~time-varying~~mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said ~~time-varying~~mixing signal φ_1 to generate an output signal $x(t)\ \varphi_1$; and

a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal $x(t)\ \varphi_1$ with said ~~time-varying~~mixing signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

2. The radio frequency (RF) up-convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for generating ~~time-varying~~mixing signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

3. The radio frequency (RF) up-convertor of claim 2 wherein said synthesizer further comprises:

a synthesizer for generating ~~time-varying~~mixing signals φ_1 and φ_2, where $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

4. The convertor of claim 3, further comprising:

a closed loop error correction circuit.

5. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal $x(t)\ \varphi_1\ \varphi_2$; and

a time-varying signal modification circuit for modifying a parameter of one of said ~~time-varying~~mixing signals φ_1 and φ_2 to minimize said error level.

6. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a power measurement.

7. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a voltage measurement.

8. The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a current measurement.

9. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the phase delay of one of said ~~time-varying~~mixing signals φ_1 and φ_2.

10. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the fall or rise time of one of said ~~time-varying~~mixing signals φ_1 and φ_2.

11. The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said ~~time-varying~~mixing signals φ_1 and φ_2.

12. The radio frequency (RF) up-convertor of claim 3 wherein said synthesizer further comprises:
a synthesizer for generating ~~time-varying~~mixing signals φ_1 and φ_2, where said ~~time-varying~~mixing signals φ_1 and φ_2 can change with time in order to reduce errors.

13. The radio frequency (RF) up-convertor of claim 3, further comprising:
a DC offset correction circuit.

14. The radio frequency (RF) up-convertor of claim 13, wherein said DC offset correction circuit comprises:
a DC offset generating circuit for generating a DC offset voltage;
a summer for adding said DC offset voltage to an output of one of said mixers; and

a DC error level measurement circuit for modifying the level of said DC offset voltage to minimize error level.

15. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a power measurement circuit.

16. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a voltage measurement circuit.

17. The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a current measurement circuit.

18. The radio frequency (RF) up-convertor of claim 1, further comprising:
a filter for removing unwanted signal components.

19. The radio frequency (RF) up-convertor of claim 18, ~~further comprising~~where said filter comprises:
a filter for removing unwanted signal components from said *x(t)* φ_1 signal.

20. The radio frequency (RF) up-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are random.

21. The radio frequency (RF) up-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are pseudo-random.

22. The radio frequency (RF) up-convertor of claim 1, wherein said ~~time-varying signals are irregular~~synthesizer uses a single time base to generate both mixing signals φ_1 and φ_2.

23. The radio frequency (RF) up-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are digital waveforms.

24. The radio frequency (RF) up-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are square waveforms.

25. The radio frequency (RF) up-converter of claim 3, further comprising:

a local oscillator coupled to said synthesizer for providing a periodic signal having a frequency that is an integral multiple of the frequency of said local oscillator signal being emulated.

26. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises a digital signal processor (DSP).

27. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises analogue components.

28. The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal *x(t)* φ_1; and

a time-varying signal modification circuit for modifying a parameter of one of said ~~time-varying~~ mixing signals φ_1 and φ_2 to minimize said error level.

29. The radio frequency (RF) up-convertor of claim 1, ~~further comprising: a filter for removing unwanted signal components~~: where said synthesizer uses different patterns to generate signals φ_1 and φ_2.

~~30. The radio frequency (RF) up-converter of claim 1, further comprising: a filter for removing unwanted signal components from said *x(t)* φ_1 signal.~~

31. A method of modulating a baseband signal *x(t)* comprising the steps of:

generating ~~time-varying~~ mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi 1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

mixing said input signal *x(t)* with said ~~time-varying~~ mixing signal φ_1; to generate an output signal *x(t)* φ_1; and

mixing said signal *x(t)* φ_1 with said ~~time-varying~~ mixing signal φ_2 to generate an output signal *x(t)* $\varphi_1 \varphi_2$.

32. An integrated circuit comprising the radio frequency (RF) up-convertor of ~~any one of claims 1-30~~ claim 1.

33. ~~A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1-30.~~

34. ~~A computer data signal embodied in a carrier wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) up-convertor of any one of claims 1-30.~~